ARGUMENTS

1. Claim rejections 35 U.S.C. 112

Claims 14-32 were rejected under 35 U.S.C. 112 as failing to comply with the written description requirement.

Claims 14-24

Claim 14 is formed by amending original Claim 1 to include the limitations of "a second buffer for buffering a second input signal and outputting a second output signal; a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and a second variable capacitor coupled to the second DAC and the second buffer; wherein by controlling at least one of the first and the second digital values, the phase difference between the first input signal and the second input signal are adjusted". This limitation is fully supported in specification paragraph [0018], where applicants write "two or more of the above-mentioned circuits of the claimed invention can also be implemented at the same time." The above-mentioned circuit of the claimed invention comprises a first DAC, a first buffer, and a first variable capacitor, wherein the circuit is utilized for generating a phase delay. It should be obvious to one skilled in the art that a second line of elements can be added directly below the circuit detailed in Fig.2, wherein a first input signal is input to the first buffer, and a second input signal is input to the second buffer. Both circuits respectively operate to generate a phase difference of a first input signal and to generate a phase difference of a second input signal. In this case, the phases of each input signal will be adjusted, thereby adjusting the phase difference between the two input signals.

Although the operation of the second line of elements is not explicitly described in the specification, the function of the second buffer is identical to the function of the first

buffer, the function of the second DAC is identical to the function of the first DAC, and the function of the second capacitor is identical to the function of the first capacitor. Each line of elements operates to adjust a phase of an input signal, but having two lines of elements allows a phase difference between two input signals to be adjusted. As such, applicants believe details of the apparatus claimed in Claim 14 are provided in specification paragraph [0018], and details provided in the specification are sufficient for one skilled in the art to clearly understand the function of the apparatus detailed in Claim 14.

As to limitations claimed in claims 18-19, these limitations are fully supported in specification paragraph [0018], where applicants write "the two input signals may be a pair of differential signals, or I/Q signals of a receiver and/or a transmitter of communication systems."

As to limitations claimed in claims 20-21, these limitations are fully supported in specification paragraph [0017], where applicants write " The input signal received by the buffer 20 is usually a clock signal outputted by a clock generator or a signal outputted by an RF transceiver."

As to limitations claimed in claims 22-24, these limitations are fully supported in specification [0017], where applicants write "the variable capacitor 22 can be a MOS-based voltage-controlled capacitor (or a varactor), or a P+/N well junction voltage-controlled capacitor."

Claims 25-32

Claim 25 is a method claim describing the operation of the apparatus claimed in Claim 14, wherein a description is given of adjusting a phase difference between two

input phase signals by respectively generating a phase delay of the first input signal and the second input signal. The method of Claim 25 involves generating a phase delay in a manner that is clearly detailed in the specification. Claim 25 merely adds the limitation that a phase delay of a second input signal can also be generated, wherein the phase delay of the second input signal is generated in a manner consistent with the way a phase delay of a first input signal is generated, as supported in the specification. Claim 25 further claims that generating a phase delay for at least one of a first input signal and a second input signal can adjust the phase difference between the first input signal and the second input signal, as is fully supported in specification paragraph [0018] "In the case of two, the two circuits can respectively adjust the phases of two input signals (one input signal per circuit) in order to adjust the phase difference between the input signals". Applicants therefore believe detail provided in the specification, of both the method of generating a phase delay for an input signal, and the method for adjusting a phase difference between two input signals by generating a phase delay for at least one of the input signals, is sufficient to place Claim 25 in a position for allowance.

Since claims 26-32 correspond to claims 18-24, respectively, it is obvious that limitations claimed in claims 26-32 are fully supported by original specification.

In summary, claims 14-32 indeed comply with the written description requirement. Reconsideration of claims 14-32 is respectfully requested. In addition, reconsideration of the finality of the last Office action is respectfully requested.

2. Patentability of claims 14-32

According to Applicants' arguments filed on 11/25/2005, Applicants believe that claims 14-32 have been placed in condition for allowance. Reconsideration of claims

14-32 is respectfully requested.

3. Claim rejections 35 U.S.C. 103(a)

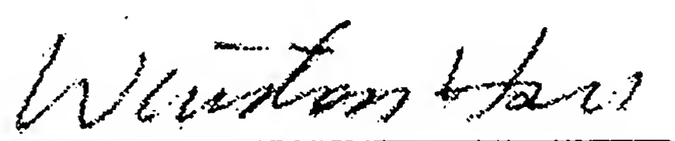
Claims 1 and 7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kameya in view of Park.

Response

Claims 1 and 7 have been cancelled.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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